Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to clarify Applicants invention.

Support for the amended claims is found in the original claims, the Figures and the Specification. No new matter has been introduced.

For example support for the amendments is found in the Figures (1B-1E) as well as in the Specification at paragraph 0030:

"At this point, after forming a respective tensile stress dielectric layer e.g., 24A over the NMOS device and a compressive stress dielectric layer e.g., 24B over the PMOS device, an annealing process is not necessary if the respective dielectric layers will remain in place to form a protective layer, e.g., a contact etching stop layer in subsequent processes. On the other hand, if the stressed dielectric layers 24A and 24B are desired to be removed **to improve a subsequent gap filling process**, prior to removal, an annealing process, similar to that previously outlined is preferably carried out to

recrystallized amorphous polysilicon portions with the respective stressed dielectric layers in place over one or both of the NMOS and PMOS devices to transfer a stress to the channel region to form a strained channel thereby improving the charge carrier mobility in at least one and preferably both NMOS and PMOS devices."

And at paragraph 0032:

"Referring to Figure 1F, in a another embodiment, if the dielectric layer portions 24A and 24B are removed, and oxide buffer layer 23, **conventional processes may then carried out to complete formation of the NMOS and PMOS MOSFET devices including forming salicide** (self aligned silicide) portions over the source and drain regions e.g., 28A and 28B, and silicide over the upper portion of the polysilicon electrodes, e.g., 30A and 30B."

And at paragraph 0034:

"Among the several advantages of the invention include the fact that the **stressed dielectric layer may be deposited at higher temperatures since the deposition temperature is limited by a temperature of amorphous polysilicon recrystallization rather than another phase transformation such as a previously formed salicides.**"

Claim Rejections under 35 USC 102

Claims 1-30 stand rejection under 35 USC 102(e) as being

anticipated by Chidambarrao et al. (US 6, 890,808).

Chidambarrao et al. disclose a process for selectively introducing strain (stress) into a substrate (channel region) by the formation of metal silicide on the top portions of polysilicon gate electrodes (see Abstract; col 2, lines 1-38)). The process involves the formation gate electrodes including the formation of sidewall spacers and silicide regions (see Fig 2d-2e, item 34;col 4, lines 59-col 5, line 5), followed by forming an oxide fill (item 35 Figure 2e) between gate electrodes, followed by a CMP process to expose top polysilicon gate portions (col 5, lines 6-8), followed by over etching the P-type polysilicon gate top portion (col 5, lines 8-10), followed by deposition of another metal on the top portion of the polysilicon gates (col 5, lines 25-32), followed by an annealing process to form a metal silicide (col 5, lines 32-37, item 40, Figure 2(h) on the top portion of the gates, to selectively form stresses in the underlying channel regions (substrate) (col 2, lines 14-18).

Thus, Chidambarrao et al. disclose a significantly different process for forming stress in the substrate (overetched polysilicon gates) and fail to disclose several aspects of Applicants disclosed and claimed invention including:

"forming a first strained layer with a first type of stress overlying said first gate including gate sidewall portions; and,

forming a second strained layer with a second type of stress overlying said second gate including gate sidewall portions."

In the method of Chidambarrao et al., Chidambarrao et al. uses overetched polysilicon gates to create compressive stresses in the channel region of the PFETs and tensile stresses in the NFET channel region due to a difference in the gate heights and confinement by the gap fill layers rather than a difference in types of strain of the strained layers (see col 2, lines 57-67; col3, lines 7-20); i.e., the same strained layer (silicide) is formed only over only a top portion of an n and P type gate electrodes formed at different heights.

Thus, Chidambarrao et al. fail to disclose a first and second strained layer with a respective first and second stress type and do not disclose forming the layers over gate sidewall portions.

Likewise, Chidambarrao et al. fail to disclose Applicants

elements in independent claims 15-17 and 21.

With respect to claims 5 and 6, 16, 17, 18, and 29 nowhere do Chidambarrao et al. disclose "forming an amorphous portion in the first and second gates" or "recrystallizing the amorphous portion".

With respect to claims 8, 15, 16, 20, and 21, nowhere do Chidambarrao et al. disclose Applicants claimed and disclosed steps, but rather discloses removing both of the first metal silicides from the top portion of the polysilicon by a CMP process to form two uncovered portions, followed overetching the P-type gate, followed forming a second silicide over the top portions of gates.

With respect to claims 10, 11, 23, and 24, nowhere do Chidambarrao et al. disclose that the strained layer is a dielectric layer or a nitride, silicon nitride or silicon oxynitride as Applicants disclose and claim, but rather, Chidambarrao et al. disclose the strained layer is a **metal silicide**. The only reference in Chidambarrao et al. to silicon nitride is with respect to formation of a pad silicon nitride

layer in the formation of isolation trenches and formation of silicon nitride spacers (col 3, lines 63-64; col 4, lines 41-45).

Thus, Chidambarrao et al. is clearly insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Thus, the cited reference fails to make out a *prima facie* case of anticipation with respect to Applicants independent claims, and therefore Applicants dependent claims.

Based on the foregoing, Applicants submit that the Claims are in condition for allowance. Such favorable action by the Examiner

at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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